Electronic Version
Stylesheet Version v1.1.1

[A SYSTEM AND METHOD OF PROVIDING ERROR DETECTION AND CORRECTION CAPABILITY IN AN INTEGRATED CIRCUIT USING REDUNDANT LOGIC CELLS OF AN EMBEDDED FPGA]

Abstract

A system and method of providing error detection and correction capability in an IC using redundant logic cells and an embedded field programmable gate array (FPGA). The system and method provide error correction (EC) to enable a defective logic function implemented within an IC chip design to be replaced, wherein at least one embedded FPGA is provided in the IC chip to perform a logic function. If a defective logic function is identified in the IC design, the embedded FPGA is programmed to correctly perform the defective logic function. All inputs in an input cone of logic of the defective logic function are identified and are directed into the embedded FPGA, such that the embedded FPGA performs the logic function of the defective logic function. All outputs in an output cone of logic of the defective logic function are identified,

and the output of the FPGA is directed to the output cone of logic of the defective logic function, such that logic EC is provided within the embedded FPGA structure of the IC chip.